

## CLAIMS

1. A fluid ejection device comprising:
  - a fire line configured to receive an energy signal having energy pulses;
  - a drive switch configured to control the energy signal to eject fluid;
  - a first transistor having a first gate configured in a first loop structure;
  - a second transistor having a second gate configured in a second loop structure; and
  - a third transistor having a third gate configured in a third loop structure disposed around the first transistor, wherein the second transistor and the third transistor share a first active region, and wherein the first transistor and at least one of the second and third transistors are configured to control the drive switch.
2. The fluid ejection device of claim 1, wherein the second transistor and the third transistor are configured to control the drive switch.
3. The fluid ejection device of claim 1, wherein one of the second and third transistors is a guard transistor.
4. The fluid ejection device of claim 1, comprising:
  - a fourth transistor having a fourth gate configured in a fourth loop structure, wherein the second transistor and the fourth transistor share a second active region and the first gate is disposed around a third active region that is electrically coupled to the second active region.
5. The fluid ejection device of claim 4, wherein the fourth gate is disposed around a fourth active region that is configured to receive a signal to charge the second active region and the third active region.
6. The fluid ejection device of claim 1, comprising:

a fourth transistor having a fourth gate configured in a fourth loop structure, wherein the second transistor and the fourth transistor share a second active region.

7. The fluid ejection device of claim 6, wherein the fourth gate is disposed around a third active region and the first gate is disposed around a fourth active region that is electrically coupled to the third active region.

8. The fluid ejection device of claim 7, wherein the second active region is configured to receive a signal to charge the third active region and the fourth active region.

9. The fluid ejection device of claim 1, comprising:

a fourth transistor having a fourth gate configured in a fourth loop structure, wherein the second gate is disposed around the fourth transistor.

10. The fluid ejection device of claim 1, wherein the third gate is disposed around the second transistor.

11. The fluid ejection device of claim 1, wherein the third gate is disposed around the second transistor and the first gate is within the second gate.

12. The fluid ejection device of claim 1, wherein the second gate is disposed around the third transistor.

13. The fluid ejection device of claim 1, wherein the first transistor and the second transistor share the first active region.

14. The fluid ejection device of claim 1, wherein the first transistor and the second transistor share the first active region and the first gate is disposed around a second active region that is configured to receive a signal to charge the first active region.

15. The fluid ejection device of claim 14, wherein the second gate is disposed around a third active region that is coupled to data/address transistors and the first active region is coupled to the drive switch.

16. The fluid ejection device of claim 1, wherein the first transistor and the third transistor share the first active region.

17. The fluid ejection device of claim 1, wherein the first transistor and the second transistor share a second active region.

18. The fluid ejection device of claim 1, wherein the first transistor and the third transistor share a second active region.

19. A device comprising:  
a first transistor having a first gate configured in a first loop structure;  
a second transistor having a second gate configured in a second loop structure; and  
a third transistor having a third gate configured in a third loop structure, wherein the first transistor and the second transistor are disposed within the third gate.

20. The device of claim 19, wherein the first transistor and the third transistor share an active region.

21. The device of claim 19, wherein the first transistor, the second transistor and the third transistor share an active region.

22. The device of claim 19, wherein the first transistor, the second transistor and the third transistor share a first active region and the first gate is disposed around a second active region that is configured to receive a signal to charge the first active region.

23. The device of claim 19, comprising:

a drive switch, wherein the first transistor, the second transistor and the third transistor share a first active region that is coupled to the drive switch and the first gate is disposed around a second active region that is coupled to data/address transistors.

24. A device, comprising:

a substrate having a first active region and a second active region;  
a first gate configured in a first loop structure around the first active region;  
a second gate configured in a second loop structure around the second active region; and  
a third gate configured in a third loop structure around the first gate and the second gate.

25. The device of claim 24, wherein the first active region is isolated from the second gate and the second active region is isolated from the first gate.

26. The device of claim 24, wherein the substrate has a third active region and the third gate is disposed around the third active region, wherein the third active region is in contact with the first gate and the second gate.

27. A device comprising:

a first transistor having a first gate configured in a first loop structure;  
a second transistor having a second gate configured in a second loop structure;  
a third transistor having a third gate configured in a third loop structure;  
and  
a fourth transistor having a fourth gate configured in a fourth loop structure, wherein the first transistor is disposed within the second gate and the third transistor is disposed within the fourth gate.

28. The device of claim 27, wherein the second transistor and the fourth transistor share an active region.
29. The device of claim 27, wherein the first gate is disposed around a first active region and the fourth gate is disposed around a second active region that is electrically coupled to the first active region.
30. The device of claim 29, wherein the third gate is disposed around a third active region configured to receive a signal to charge the first active region and the second active region.
31. The device of claim 27, wherein the first gate is disposed around a first active region and the third gate is disposed around a second active region that is electrically coupled to the first active region.
32. The device of claim 31, wherein the fourth gate is disposed around a third active region configured to receive a signal to charge the first active region and the second active region.
33. A device, comprising:  
a substrate having a first active region, a second active region and a third active region;  
a first gate configured in a first loop structure around the first active region;  
a second gate configured in a second loop structure around the second active region; and  
a third gate configured in a third loop structure around the third active region, wherein the second active region is electrically coupled to the third active region.

34. The device of claim 33, wherein the first gate is disposed around the second gate.

35. The device of claim 33, wherein the substrate has a fourth active region and comprising:

a fourth gate configured in a fourth loop structure around the fourth active region, wherein the first gate is disposed around the second gate and the third gate is disposed around the fourth gate.

36. A device comprising:

a first transistor having a first gate, a first active region and a second active region, wherein the first gate is configured in a first loop structure around the first active region; and

a second transistor having a second gate configured in a second loop structure around the second active region, wherein the second active region and the first gate are configured to receive a first signal and the first active region is configured to provide a second signal in response to the first signal.

37. The device of claim 36, wherein the first active region is configured to provide a lower capacitance than the second active region.

38. A method of controlling fluid ejection from a fluid ejection device, the method comprising:

receiving energy pulses;

controlling a drive switch with a first transistor having a first gate configured in a first loop structure, a second transistor having a second gate configured in a second loop structure, and a third transistor having a third gate configured in a third loop structure disposed around the first transistor, wherein the second transistor and the third transistor share a first active region; and

controlling, with the drive switch, the energy pulses to eject fluid.

39. The method of claim 38 further comprising:

.controlling the drive switch with a fourth transistor having a fourth gate configured in a fourth loop structure, wherein the second transistor and the fourth transistor share a second active region and the first gate is disposed around a third active region that is electrically coupled to the second active region.

40. The method of claim 39 further comprising:

receiving, with a fourth active region, a signal to charge the second active region and the third active region, wherein the fourth gate is disposed around the fourth active region.

41. The method of claim 38 further comprising:

controlling the drive switch with a fourth transistor having a fourth gate configured in a fourth loop structure, wherein the second transistor and the fourth transistor share a second active region.

42. The method of claims 41, wherein the fourth gate is disposed around a third active region and the first gate is disposed around a fourth active region that is electrically coupled to the third active region.

43. The method of claim 38, wherein the third gate is disposed around the second transistor.

44. The method of claim 38, wherein the first transistor and the second transistor share the first active region.